# Improved Dynamic Shape Representation Using a Biologically-Inspired Vision Sensor with a Synchronous Arbitration

A.N. Belbachir, *Member IEEE*, M. Hofstätter, M. Litzenberger and P. Schön

Austrian Research Centers GmbH - ARC

smart systems Division

Donau-City-Strasse 1 -1220, Vienna, Austria
{ahmed.belbachir, michael.hofstaetter, martin.litzenberger, peter.schoen}@arcs.ac.at

Abstract— Neuromorphic temporal contrast vision sensors are sensitive to relative intensity changes. These sensors can be exploited to detect scene dynamics and representing the resulting dynamic's shapes. Moreover, these sensors are ideal for ultra-high-speed vision with low computational effort. Two aspects have been ignored within the initial conceptual design of this kind of sensors: the preservation of the high temporal resolution of the pixels' data and handling high peak rates. In other words, timestamping the pixels' data and the minimization of the data loss in case of pixel spiking at higher rate have not been intensively investigated. This work provides an on-chip solution using a synchronous Address-Event interface for maintaining the precise temporal information and reducing the data loss for high-speed applications.

#### I. Introduction

Biologically-inspired vision aims to duplicate the effect of human vision by electronically capturing, perceiving and understanding images. Introduced in the late 80's, neuromorphic engineering is tremendously evolving with the enduring motivation in rebuilding part of the human vision mechanism in low-cost and low power electronics. The main concern of these systems is the representation of information by the relative values of analogue signals, rather than by the absolute values of digital signals as argued by Carver Mead in the invited paper [12].

Vision models have been built in sensors like the one of Mahowald and Mead [10] [11], originally named the "silicon retina" sensor. In succession, a large variety of diverse silicon-retina sensor designs have been carried out and reported, including gradient based sensors sensitive to static edges [6], temporal contrast vision sensors that are sensitive to relative light intensity changes [8][13], orientation selective spiking neurons devices [9] from Tobi Delbrück and its group in ETH Zürich and optical flow sensors [4] from Bernabe Linares-Barranco.

Temporal contrast vision sensors focused in this paper feature massively parallel pre-processing of the visual information on-chip analogue circuits and are commonly characterized by high temporal resolution, wide dynamic range and low power consumption. Each pixel operates autonomously and responds with low latency to relative illumination changes by generating asynchronous events [13]. It generates two types of events, which represent a fractional increase or decrease in light intensity that exceeds a tunable threshold. Combined with the pixel address, these events are referred to as 'Address-Events' (AE) [5]. Unlike clocked CMOS vision sensors, neuromorphic imagers require an arbiter to organize the access of multiple asynchronous data sources (pixels) to a common communication bus. As the pixels are autonomous, several pixels can generate AE instantaneously and therefore, the AE interface (arbiter) is needed to arbitrate the transfer of concurrent events the temporally via communication bus.

K.A. Boahen [2][3] has developed AE communication circuits for the events transmission. This asynchronous AE interface handles temporally coincident pixels' events for up to  $10^6$  AE/ second. However, the digital timing information is not allocated to AE on-chip and has to be provided in an external unit (e.g. from the processing unit). Furthermore, the arbitration process is not deterministic because of the unfettered design of this AE communication circuit.

For this reason, we have developed a synchronous AE interface [7] for deterministically arbitrating between multiple asynchronous sensor elements and adding a timestamp to the AE at the generation time, for preserving ultra-high precision temporal information. Both arbiters [2] and [7] have been implemented in the temporal contrast vision dual-line sensor chip [13] where only one of them can be activated at a time in the data acquisition phase.

This paper presents a comparative study between the asynchronous and synchronous AE communication interfaces implemented in the dual-line sensor chip. Furthermore, this paper shows the advantage of the synchronous arbitration in representing ultra high-speed dynamics and moving objects as well as preserving the high

temporal resolution of the pixels' data. The paper is structured as follows. In Section II, the characteristics of the AE communication interfaces (asynchronous and synchronous) are summarized. Section III presents a performance analysis of the dual-line sensor using both arbiters (asynchronous and synchronous). The experimental results using both AE communication interfaces in capturing high-speed moving objects are presented in Section IV. A summary and discussions are given in Section V.

#### II. ADDRESS-EVENTS COMMUNICATION INTERFACE

In this Section, the characteristics of both AE communication interfaces, asynchronous and synchronous, implemented in the dual-line sensor are given.

#### A. Asynchrnous Address-Event Interface

The pixels handshake asynchronously with the peripheral circuits and communicate their address and the type of event (ON: for intensity increase and OFF: for intensity decrease). The pixels' data are transferred via a shared communication bus. Therefore, an AE communication interface [2] aims to lossless transmit all AE in arbitrating between temporally coincident events. The asynchronous AE circuits of the dual-line sensor are based on the ones described in [2].

The time information is allocated to the events off-chip, in the processing unit. Therefore, the timing accuracy of AE strongly depends on the performance of the arbitration and on the stimulus-driven spatio-temporal activity; a fast stimulus may yield a bulk of events from coincident pixels saturating the arbiter.

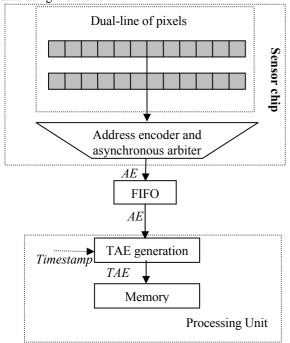


Fig. 1. Communication periphery including the asynchronous address-event interface

Fig. 1 depicts the process of generating data using the asynchronous arbiter implemented in the dual-line sensor. The data are encoded into AE and arbitrated for coincident pixel activities at the pixel interface. The time information is assigned in the processing unit and the resulting data is called Timed AE (TAE). These data consist of timestamps and AE. They are stored in the memory and are ready for further processing.

#### B. Synchronous Address-Event Interface

In addition to arbitrating between coincident pixels events, the synchronous arbiter [7] performs the timestamp assignment with respect to the occurrence of an event at the arbiter input. They are generated using a continuous counting device while assigning the current counter value to the events. The timestamps are combined with the corresponding AE to compose a stream of data packets, which are called TAE at the output of the arbiter. Events with the same timestamp value are interpreted as concurrent and they are arbitrated according to descending addresses.

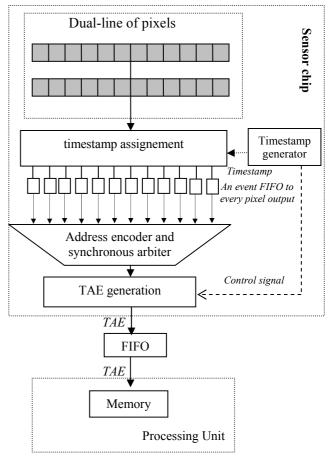


Fig. 2. Communication periphery including the synchronous address-event interface

Fig. 2 presents the process of generating TAE using the synchronous arbiter implemented in the dual-line sensor. A timestamp is attached on-chip to the AE data with a temporal resolution of 100ns at the input stage of the arbiter. Therefore, the output of the sensor consists of TAE with the AE and their accurate occurrence time. In order to avoid data loss, an event FIFO is build at the output of every pixel in order to handle peak data rates and to allow storing the pixels' data whenever the synchronous arbiter is temporary computationally saturated.

Both arbiters have been implemented in a standard 0.35  $\mu m$  CMOS process.

The asynchronous AE interface has an area penalty of about 7.5% while the synchronous AE interface covers 31% of the whole chip area. Indeed, by including the timestamp generator and the event FIFOs, the AE interface requires more space. However, by using digital CMOS technology  $(0.18\mu m)$ , the synchronous AE interface area will shrink by 80%.

#### III. PERFROMANCE ANAYLSIS

The dual-line sensors chip [13] has implemented the arbitration concepts: asynchronous arbiter and synchronous arbiter as digital circuits, to handle temporally coincident pixels' events. Only one arbitration concept can be active at a time. The dual-line sensor consists of two lines of 256 autonomous pixels, which asynchronously respond to relative illumination changes. The sensor performance using the asynchronous and synchronous arbiter as summarized in TABLE I.

TABLE I. DUAL-LINE SENSOR PERFROMANCE ANALYSIS USING THE ASYNCHRNOUS AND THE SYNCHRNOUS ARBITER

Characteristics	Asynchronous Arbiter	Synchronous Arbiter
Arbitration behavior	Not deterministic	Deterministic (pixel address in a descending order per timestamp)
Data organization	Random	Timestamp + pixel addresses in decreasing order
On-chip temporal resolution	No time quantization	≥ 100ns
Peak input data rate	10 <sup>6</sup> Event/s	2.56 10 <sup>9</sup> Event/s @20 MHz system clock frequency
Peak output data rate	10 <sup>6</sup> Event/s	10 <sup>7</sup> Event/s @20 MHz system clock frequency
Handling of Peak data rate	None	Event FIFOs included to minimize data loss and to maintain the temporal information
Possibility for pixel masking	No	Yes
Clock frequency	No clock	10 – 40 MHz

From the analysis of the theoretical characteristics of the asynchronous and the synchronous arbiters, it can be noticed that the asynchronous arbiter arbitration behavior is not deterministic and the temporal information is not preserved within the AE interface. However, the synchronous arbiter includes the time information to the AE and thus preserves the high temporal resolution aspect of the pixels. This advantage has a consequent influence on the dual-line sensor performance in capturing high-speed moving objects by preserving the object shape. The experimental evaluation of both arbiters is provided in the next section.

#### IV. EXPERIMENTAL RESULTS

Both communication interfaces are implemented in the dual-line sensor chip and only one interface can be activated at a time for scene capturing. For evaluating the arbitration performance, we activated the synchronous arbiter and captured a high-speed moving object in a scene. Then we activated the asynchronous arbiter and captured the same object and we compared afterwards both object representations between both acquisitions.

As a first step, both arbitration processes have been evaluated using the dual-line sensor stimulated by a pulsed laser source light, instantaneously flashing on all pixels to generate coincident events. Afterwards, the arbitration processes have been evaluated on capturing high-speed moving objects.

### A. Evaluation using High-speed Source

In the first test, a laser light flashing instantaneously on all pixels has been used in order to evaluate the arbitration performance between the coincident events. All 512 pixels  $(2\times256)$  have to instantaneously send an event as a reaction to the laser light flash. As all pixels events are temporally coincident, this test is adequate for evaluating the efficiency of both arbiter to route all the events through the shared communication bus.

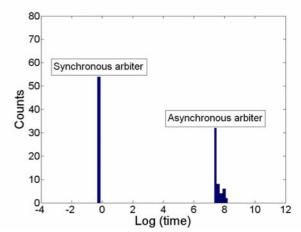


Fig. 3. Histogram of the arbitration duration with the synchronous (left) and asynchronous for several measurements

Fig. 3 depicts the statistical evaluation of the arbitration duration for several measurements with both arbiters. The x-axis (the arbitration duration) is represented in a logaritmic scale in order to plot both histograms (from the synchronous and asynchronous arbiters in one figure). The synchronous arbiter shows a systematic arbitration duration of of 0.8  $\mu s$  while the asynchronous arbiter lies between 1.6 ms and 3.5 ms in handling all 512 coincident events.

## B. Evaluation on Capturing High-Speed Moving Objects

In this test, objects crossing the sensor field of view at ultra high-speed are used for evaluating the synchronous arbitration process. Several 2-D objects have been fixed on a rotating drum with velocity greater than 15 m/s, and the corresponding AE data have been generated. The main evaluation criterion is the capturing and high-speed object representation performance of the dual-line sensor using the synchronous AE interface. Fig.4 shows an original object (Top) and its AE representation at a velocity of 25 m/s using the dual-line sensor with activated synchronous arbiter (Bottom). The synchronous arbiter supports the temporal contrast vision sensor in preserving its main advantage "the high-temporal resolution" in efficiently handling concurrent AE and thus supporting high-speed applications.

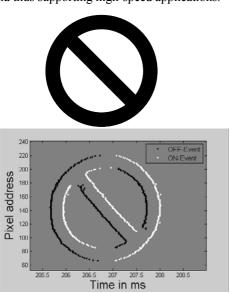


Fig. 4. Original object (top) and its AE representation using the dual-line sensor with synchronous arbitration (bottom)

The synchronous arbitration efficiently handles coincident pixels events with high accuracy and minimal data loss that maintain the original shape structure. Moreover, due to the deterministic behavior of the synchronous arbitration, the data stream with sorted AE is advantageous for vision applications in terms of algorithmic efficiency.

#### V. CONCLUSIONS

This paper presents performance analysis experimental evaluation of the synchronous and the asynchronous arbitration of temporal concurrent pixels events for biologically-inspired (neuromorphic) vision systems. Including a timestamp assignment process and an event FIFO for every pixel on-chip, the synchronous address-event interface preserves the fundamental advantage for neuromorphic temporal contrast vision sensors that is the ultra-high temporal resolution of the pixel activities, to make the system attractive for high speed vision applications. Furthermore, the synchronous arbitration process is deterministic and offers possibility to handle higher peak rates than those for the asynchronous arbiter and thus yield to minimal data loss. Moreover, this synchronous address-event interface and its digital integration allow masking and unmasking pixels in the array to adapt the sensor to different applications.

#### REFERENCES

- A.N. Belbachir, M. Litzenberger, C. Posch and P. Schön, "Real-Time Vision Using a Smart Sensor System," in the International Symposium on Industrial Electronics, ISIE2007, Spain, June 2007.
- [2] K. A. Boahen, "Point-to-point connectivity between neuromorphic chips using address events," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 47, no. 5, pp. 416–434, May 2000.
- [3] K. A. Boahen, "A burst-mode word-serial address-event link—I: Transmitter design," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 51, no. 7, pp. 1269–1280, Jul. 2004.
- [4] J. Costas-Santos, T. Serrano-Gotarredona, R. Serrano-Gotarredona and B. Linares-Barranco, "A Spatial Contrast Retina with On-chip Calibration for Neuromorphic Spike-Based AER Vision Systems," IEEE Trans. CAS, vol. 54, No. 7, pp. 1444-1458, July 2007.
- [5] E. Culurciello, R. Etienne-Cummings, K. Boahen, "Arbitrated Address Event Representation Digital Image Sensor," ISSCC Dig. Tech. Papers, pp. 92–93, Feb. 2001
- [6] T. Delbrück, "Silicon Retina with Correlation-Based, Velocity-Tuned Pixels," IEEE Trans. Neural Netw., Vol. 4, No. 3, pp. 529-541, 1993.
- [7] M. Hofstätter, A.N. Belbachir, E. Bodenstorfer and P. Schön, "Multiple Input Digital Arbiter with Timestamp Assignment for Asynchronous Sensor Arrays," IEEE ICECS06, Nice, France, 2006.
- [8] P. Lichtsteiner, C. Posch and T. Delbrück, "A 128×128 120dB 15us Latency Asynchronous Temporal Contrast Vision Sensor," IEEE Journal of Solid State Circuits, Vol. 43, pp. 566 - 576, Feb. 2008.
- [9] S.-C. Liu, J. Kramer, G. Indiveri, T. Delbrück, T. Burg, and R. Douglas, "Orientation-selective aVLSI spiking neurons," Neural Networks, Special Issue on Spiking Neurons in Neuroscience and Technology, 14(6/7), pgs 629-643, 2001.
- [10] M. A. Mahowald and C. A. Mead, "A Silicon Model of Early Visual Processing," Neural Networks, vol. 1, pp. 91-97, 1988.
- [11] M. A. Mahowald and C. A. Mead, "Silicon Retina," in C. A. Mead, Analog VLSI and Neural Systems. Reading, pp. 257-278, MA: Addison-Wesley, 1989.
- [12] C. Mead, "Neuromorphic Electronic Systems," Proceedings of the IEEE Volume 78, Issue 10 pp. 1629-1636, Oct 1990
- [13] C. Posch, M. Hofstätter, D. Matolin, G. Vanstraelen, P. Schön, N. Donath and M. Litzenberger, "A Dual-Line Optical Transient Sensor with On-chip Precision Timestamp Generation," IEEE International Conference on Solid-State Circuits, USA, February 2007.