High-Precision Timestamping and Ultra High-Speed Arbitration of Transient Pixels' Events

A.N. Belbachir, *Member IEEE,* M. Hofstätter, K. Reisinger, M. Litzenberger and P. Schön
Austrian Research Centers GmbH - ARC
smart systems Division
Donau-City-Strasse 1 -1220, Vienna, Austria
{ahmed.belbachir, michael.hofstaetter, karl.reisinger, martin.litzenberger, peter.schoen}@arcs.ac.at

***Abstract*— In this article, an ultra high-speed arbitration process for transient pixels' data is presented. Enabling a high-precision timestamping, this system demonstrates its uniqueness for handling high peak rates and preserving the main advantage of the neuromorphic electronic systems, that is high and accurate temporal resolution. Based on synchronous arbitration concept, the timestamping has accuracy better than 1 μs. The performance analysis in several tests and concept advantages over asynchronous arbitration are also discussed.**

I. INTRODUCTION

Neuromorphic electronics have recently shown an emerging interest owing to their low-cost and low power advantages as well as to the enduring motivation in rebuilding part of the human vision mechanism. The main concern of these systems is the representation of information by the relative values of analogue signals, rather than by the absolute values of digital signals as argued by Carver Mead in the invited paper [12].

Vision models have been built in sensors like the one of Mahowald and Mead [10] [11], originally named the "silicon retina" sensor. In succession, a large variety of diverse silicon-retina sensor designs have been carried out and reported, including gradient based sensors sensitive to static edges [6], temporal contrast vision sensors that are sensitive to relative light intensity changes [8][13], orientation selective spiking neurons devices [9] from Tobi Delbrück and its group in ETH Zürich and optical flow sensors [4] from Bernabe Linares-Barranco.

The temporal contrast vision sensors focused in this paper feature massively parallel pre-processing of the visual information on-chip analogue circuits and are commonly characterized by high temporal resolution, wide dynamic range and low power consumption. Each pixel operates autonomously and responds with low latency to relative illumination changes by generating asynchronous events [13]. It generates two types of events, which represent a fractional increase or decrease in light intensity that exceeds a tunable threshold. Combined with the pixel address, these events are referred to as 'Address-Events' (AE) [5]. Unlike frame-based CMOS sensors, neuromorphic imagers require an arbiter to organize the access of multiple asynchronous data sources (pixels) to a common communication bus. As the pixels are autonomous, several pixels can generate AE instantaneously and therefore, the AE interface (arbiter) is needed to arbitrate the transfer of temporally concurrent events via the common communication bus.

K.A. Boahen [2][3] has developed AE communication circuits for the events transmission. This asynchronous AE interface handles temporally coincident pixels' events for up to 10^6 AE/ second. However, the digital timing information is not on-chip allocated to AE and has to be provided in an external unit (e.g. from the processing unit). Furthermore, the arbitration process is not deterministic because of the unfettered design of this AE communication circuit.

For this reason, we have developed a synchronous AE interface [7] for deterministically arbitrating between multiple asynchronous sensor elements and adding a timestamp to the AE at the generation time, for preserving ultra-high precision temporal information. Both arbiters [2] and [7] have been implemented in the temporal contrast vision dual-line sensor chip [13] where only one of them can be activated at a time in the data acquisition phase.

This paper presents a comparative study between the asynchronous and synchronous AE communication interfaces implemented in the dual-line sensor chip. The paper is structured as follows. In Section II, the characteristics of the AE communication interfaces (asynchronous and synchronous) are summarized. Section III presents a performance analysis of the dual-line sensor using both arbiters (asynchronous and synchronous). The experimental results using both AE communication interfaces are presented in Section IV. A summary is given in Section V.

II. ADDRESS-EVENTS COMMUNICATION INTERFACE

In this Section, the characteristics of both AE communication interfaces, asynchronous and synchronous, implemented in the dual-line sensor are given.

A. Asynchrnous Arbiter

The pixels handshake asynchronously with the peripheral circuits and communicate their address and the type of event (ON: for intensity increase and OFF: for intensity decrease). The pixels' data are transfered via a shared communication bus. Therefore, an AE communication interface [2] aims to lossless transmit all AE in arbitrating between temporally coincident events. The AE circuits of the dual-line sensor are based on the ones described in [2] but have been modified to be non-greedy like the one described in [3].

The time information is allocated to the events off-chip, in the processing unit. Therefore, the timing accuracy of AE strongly depends on the performance of the arbitration and on the stimulus-driven spatio-temporal activity; a fast stimulus may yield a bulk of events from coincident pixels saturating the arbiter.

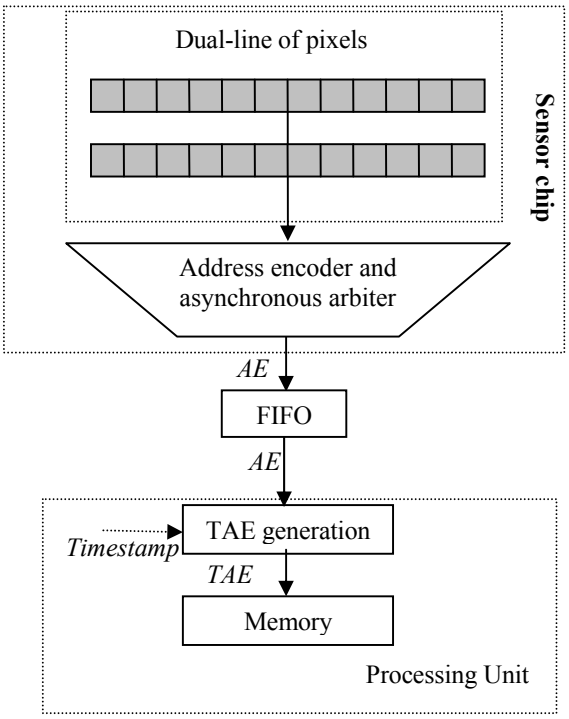


Fig. 1. Address-Event communication periphery using the asynchronous arbiter

Fig. 1 depicts the process of generating data using the asynchronous arbiter implemented in the dual-line sensor. The data are encoded into AE and arbitrated for coincident pixel activities at the pixel interface. The time information assignment occurs in the processing unit that lead to data consisting of **T**imed **AE** (TAE). These data consisting of timestamps and AE are stored in the memory and are ready for further processing.

B. Synchronous Arbiter

In addition to arbitrating between coincident pixels events, the synchronous arbiter [7] performs the timestamp assignment with respect to the occurrence of an event at the arbiter input. They are generated using a continuous counting device while assigning the current counter value to the events. The timestamps are combined with the corresponding AE to compose a stream of data packets, which are called TAE at the output of the arbiter. Events with the same timestamp value are interpreted as concurrent and they are arbitrated according to descending addresses.

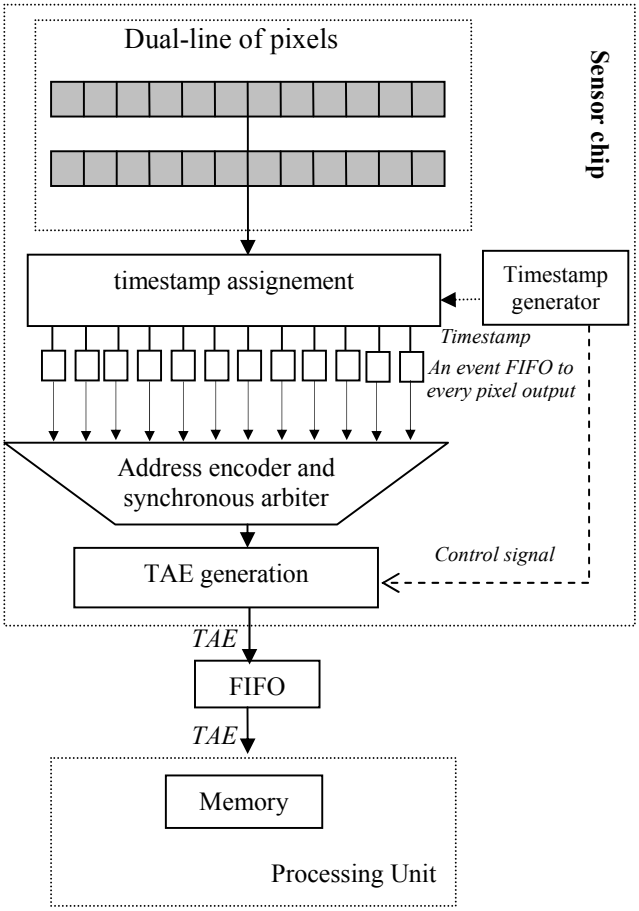


Fig. 2. Address-Event communication using the synchronous arbiter

Fig. 2 presents the process of generating TAE using the synchronous arbiter implemented in the dual-line sensor. A timestamp is attached on-chip to the AE data with a temporal resolution of 100ns at the input stage of the arbiter. Therefore, the output of the sensor consists of TAE with the AE and their accurate occurrence time. In order to avoid data loss, an event FIFO is build at the output of every pixel in order to handle peak data rates and allow storage of the pixels' data whenever the synchronous arbiter is temporary computationally saturated.

Both arbiters have been implemented in a standard 0.35 µm standard CMOS process.

III. PERFROMANCE ANAYLSIS

The dual-line sensors chip [13] has implemented the arbitration concepts: asynchronous arbiter and synchronous arbiter as digital circuits, to handle temporally coincident pixels' events. Only one arbitration concept can be active at a time. The dual-line sensor consists of two lines of 256 autonomous pixels, which asynchronously respond to relative illumination changes. The sensor performance using the asynchronous and synchronous arbiter as summarized in TABLE I.

TABLE I. DUAL-LINE SENSOR PERFROMANCE ANALYSIS USING THE ASYNCHRNOUS AND THE SYNCHRNOUS ARBITER

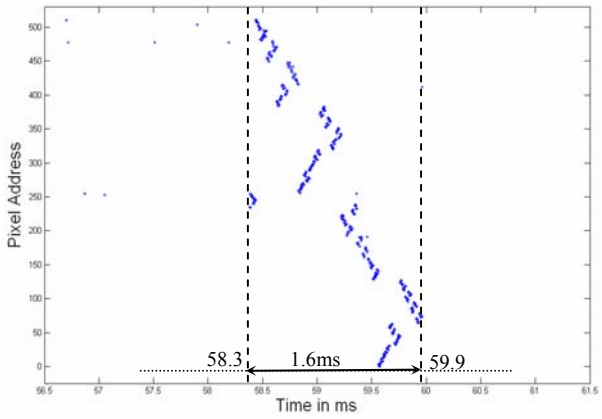
Characteristics	***Asynchronous Arbiter***	***Synchronous Arbiter***
Arbitration behavior	Not deterministic[a]	Deterministic (pixel address in a descending order per timestamp)
Data organization	Random	Timestamp + pixel addresses in decreasing order
On-chip temporal resolution	None	≥ 100ns
Peak input data rate	10^6 Event/s	2.56 10^9 Event/s @20 MHz system clock frequency
Peak output data rate	10^6 Event/s	10^7 Event/s @20 MHz system clock frequency
Handling of Peak data rate	None	Event FIFOs included to minimize data loss and to maintain the temporal information
Possibility for pixel masking	No	Yes
Clock frequency	No clock	10 – 40 MHz

A comparison between the asynchronous and the synchronous arbiters and their influence on the dual-line sensor performance shows that the asynchronous arbiter arbitration behavior is not deterministic and the temporal information is not preserved within the AE interface. However, the synchronous arbiter includes the time information to the AE and preserves the high temporal resolution aspect of the pixels.

IV. EXPERIMENTAL RESULTS

Both arbitration concepts have been evaluated using the dual-line sensor stimulated by a pulsed laser source light. In this test, a laser light flashing instantaneously on all pixels has been used in order to evaluate the arbitration performance between the coincident events. The latency of the laser light flashing is less than 30 ns and thus far below the pixel latency (~ 1µs) such that it does not affect the evaluation credibility. In order to achieve the same contrast change for all pixels, a light diffuser is used between the laser source and the dual-line sensor chip. Five milliseconds time segments are depicted in Fig.3 from the data resulting from the dual-line sensor test using the asynchronous and synchronous arbiter. The absolute time values are not equivalent as both tests have not been synchronized.

a.) Results using the asynchronous arbiter



b.) Results using the synchronous arbiter

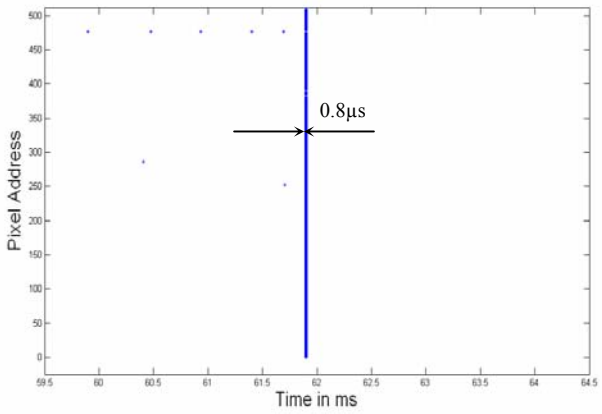


Fig. 3. Dual-line sensor data for the laser light flash using a.) the asynchronous arbiter and b.) the synchronous arbiter

In this test, all 512 pixels (2×256) have to instantaneously send an event as a reaction to the laser light flash. As all pixels events are temporally coincident, this test is adequate for evaluating the efficiency of both arbiter to route all the events to the shared communication bus. The x-axis in the figures of (Fig. 3) represents the time in milliseconds resolution while the y-axis represents the pixel index from 0 to 255 for the top and bottom lines of dual-line sensor. Fig.3 .a) shows that the asynchronous arbiter requires 1.6 ms to handle the 512 concurrent pixel events, which seems to degrade the expected laser signal (vertical line). In contrast, the synchronous arbiter (Fig. 3.b)) is able to handle the 512

concurrent events within a time period of 0.8 µs and to transmit the data in a duration of 52 µs to the processing unit. The time used for data transmission only affects the overall latency but it has no impact on the temporal information within the events due to the separative aspect of the data transfer from the processing.

Although the pixel latency is identical for both test (with asynchronous or synchronous arbiters), the synchronous arbiter introduces an additional systematic latency for the first event because of the pipelined processing and the extra-buffering of the events in the pixel interface. This systematic delay is about 7 clock cycles (350 ns @ 20 MHz) and does not affect the high-precision aspect of the synchronous arbitration as the arbitration duration is maintained to 0.8 µs. This results show that the synchronous arbiter is at least 1000 faster than the asnychronous arbiter in handling 512 coincident pixels' events.

Fig. 4 depicts the results statistical evaluation of the arbitration duration for several measurements with both arbiters. The x-axis (the arbitration duration) is represented in a logaritmic scale in order to plot both histograms (from the synchronous and asynchronous arbiters in one figure). The synchronous arbiter shows a systematic arbitration duration of of 0.8 µs while the asynchrnous arbiter lies between 1.6 ms and 3.5 ms in handlinging all 512 coincident events.

The synchronous arbitration efficiently handles coincident pixels events with high accuracy as well as the signal structure is maintained. Moreover, due to the deterministic behavior of the synchronous arbitration, the AE data stream is advantageous for vision applications in terms of algorithmic efficiency.

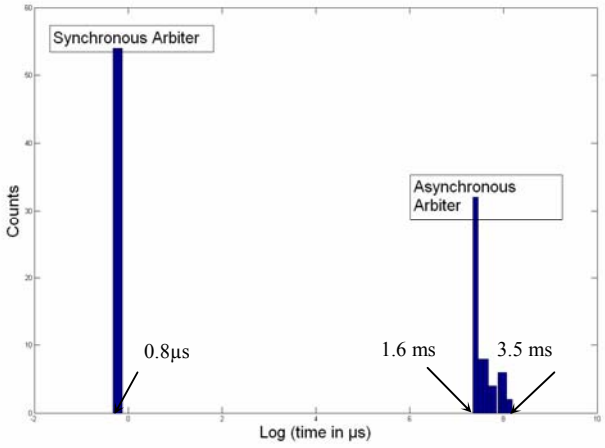


Fig. 4. Histogram of the arbitration duration with the synchronous (left) and asynchronous for several measurements

V. CONCLUSIONS

This paper presents performance analysis and experimental evaluation of the synchronous and the asynchronous arbitration of temporal concurrent pixels events for neuromorphic electronic systems. Including an on-chip timestamp assignment, the synchronous arbiter preserves the neuromorphic systems advantages in ultra-high temporal resolution as well as the temporal accuracy of the pixel activities, to make the system attractive for ultra-high speed vision applications. Furthermore, the synchronous arbiter offers possibility to handle higher peak rates than those for the asynchronous arbiter and thus yield to minimal data loss and the synchronous arbitration is at least 1000 faster than the asynchronous arbitration. Moreover, this synchronous arbiter and its digital integration allow masking and unmasking pixels in the array to adapt the sensor to different applications.

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